What is claimed is:

1. A method for fabricating a nonvolatile memory device comprising:

forming a lower insulating layer and a sacrificial layer on a semiconductor substrate;

patterning the sacrificial layer and lower insulating layer, wherein spacers are formed on sidewalls of the sacrificial layer pattern, the spacers being formed of polymers resulting from the etching of the sacrificial layer;

removing the exposed lower insulating layer to form a lower insulating layer pattern; and

removing the sacrificial layer pattern and the spacers.

2. The method as defined by claim 1, wherein the sacrificial layer is formed of nitride.

3. The method as defined by claim 1, wherein the spacers have a width between 300Å and 1000Å.

4. The method as defined by claim 1, further comprising:

forming an upper oxide layer with uniform thickness on the lower insulating layer pattern; and

forming a gate poly on the upper oxide layer.